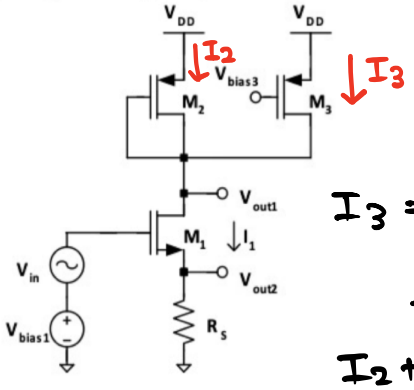
1. In the following circuit assume that all transistors are operating in the saturation region. Also, assume that $\lambda=\gamma=0$, $V_{DD}=3V$, $V_{bias3}=1.9V$, $V_{TH(NMOS)}=0.5V$, $V_{TH(PMOS)}=-0.6V$, $\mu_nC_{ox}=200\ \mu A/V^2$, $(W/L)_1 = 40$, $\mu_pC_{ox}=100\ \mu A/V^2$, $(W/L)_2 = 40$, $(W/L)_3 = 40$, and $R_S=50\Omega$.



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS}-V_{TH})^2$$

$$I_3 = \frac{1}{2}\cdot(100\times10^{-6})\cdot 40\cdot(1.9-3+0.6)^2$$

$$= 0.5mA$$

$$I_2 + I_3 = I_1$$

$$\therefore I_2 = 0.5mA$$

a) Find V_{bias1} such that the bias current of M_1 is I_1=1mA.
b) Calculate the small-signal voltage gain $A_{V1}=V_{out1}/V_{in}$.
c) Calculate the small-signal voltage gain $A_{V2}=V_{out2}/V_{in}$.
d) Calculate the small-signal output impedance seen at the output node V_{out1}.
e) Calculate the small-signal output impedance seen at the output node V_{out2}.

a) $1mA = \frac{1}{2}\cdot(200\times10^{-6})\cdot 40\cdot V_{eff_1}^2 \quad \therefore V_{eff_1} = 0.5V$

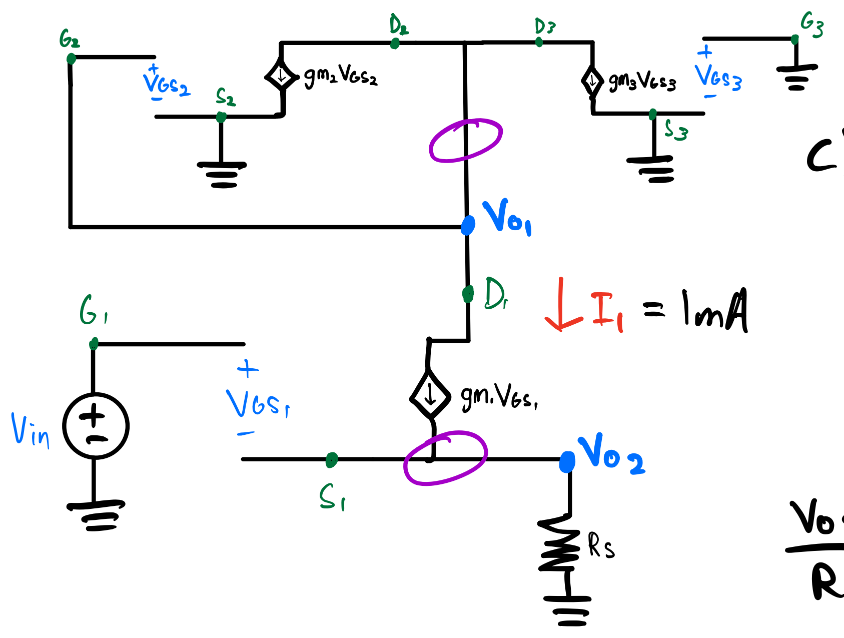
$V_{bias_1} = V_{th} + V_{eff_1} = 0.5 + 0.5 = \boxed{1V}$

Transconductance:

$$= \mu_n \cdot C_{ox}\cdot\frac{W}{L}\cdot(V_{GS}-V_{TH})$$

$$g_{m_1} = 200\cdot10^{-6}\cdot 40\cdot(0.5) = 0.004$$

Small signal Model:



$$g_{m_1}V_{GS_1} = \frac{V_{o2}}{R_S}$$

c) $V_{in} - V_{GS_1} = V_{o2}$

$$\frac{V_{o2}}{R_S} = g_{m_1}(V_{in} - V_{o2})$$

$$\frac{V_{o2}}{R_S} = g_{m_1}V_{in} - V_{o2}g_{m_1}$$

$$\frac{V_{o2}}{R_S} + V_{o2}g_{m_1} = g_{m_1}V_{in}$$

$$\frac{V_{o2}}{V_{in}} = \frac{g_{m_1}}{\left(\frac{1}{R_S}+g_{m_1}\right)} = \boxed{0.167\,V/V}$$

$V_{GS3} = 0$

$0 + V_{GS_2} = V_{o_1}$

$V_{in} - V_{GS_1} = V_{o2}$

$0 = g_{m2}V_{GS_2} + g_{m3}V_{GS3} + g_{m_1}V_{GS_1}$

$g_{m_1}V_{GS_1} = \frac{V_{o2}}{R_S}$

2. Design a common-source amplifier with a current source load based on the topology shown below with the following design specifications:

- V_{DD}=3 V
- Total power consumption of 1.5 mW
- Peak to peak output signal swing of 2.5 V
- Absolute value of gain of 40
- L = 0.4 µm for all the devices

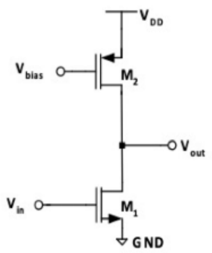
Use the following assumptions for your design

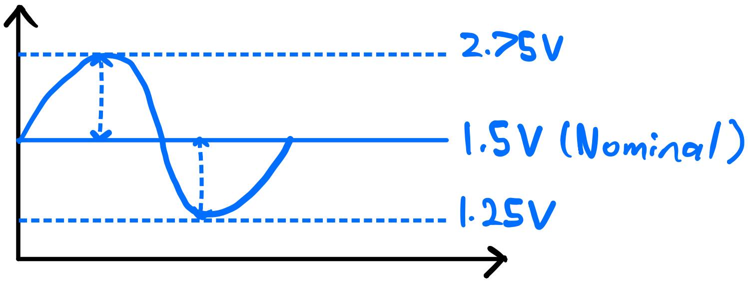
- The nominal dc level of the output node is 1.5 V

The technology parameters are:

$\lambda_{(NMOS)}$ = 0.1 V^{-1}, $\lambda_{(PMOS)}$ = 0.1 V^{-1}, γ = 0, $V_{TH(NMOS)}$ = 0.5V and $V_{TH(PMOS)}$ = -0.5V, $\mu_n C_{ox}$ = 0.2 mA/V^2, $\mu_p C_{ox}$ = 0.1 mA/V^2.

Note: Use the parameter λ only for calculating the small-signal output resistance (r_o) of the transistors. Do not use λ in any other calculation including the bias current calculations.





Find V_{bias}, DC level of the input, the transistor widths (i.e., W_1 and W_2), and the gain of the circuit.

$V_{oMax} \rightarrow V_{DG_2} < |V_{th}|,\ V_{DGMax} = |V_{th}|$

$V_{bias} = 2.75V - 0.5V = 2.25V$

$V_{omin} \rightarrow V_{GD_1} < |V_{th}|,\ V_{GDmin} = |V_{th}|$

$V_{in} = V_{G_1} = 0.5V + 0.25V = 0.75V$

Transistors are connected,

So $I_{D1} = I_{D2} = I_D$

$$\frac{1}{2}\cdot(0.2\times10^{-3})\cdot\left(\frac{W}{L}\right)_1\cdot(0.75-0.5)^2 = \frac{1}{2}\cdot(0.1\times10^{-3})\cdot\left(\frac{W}{L}\right)_2\cdot(3-2.25-0.5)^2$$

$L = 0.4\mu m$ $\quad$ $0.4\mu m$

$W_1 = 32\mu m$ $\quad$ $W_2 = 2\times W_1 = 64\mu m$

$$\frac{V_o}{V_{in}} = -g_{m_1}(r_{o1}\|r_{o2})$$

$$= -g_{m_1}\left(\frac{1}{\lambda I_{D1}}\Big\|\frac{1}{\lambda I_{D2}}\right)$$

$$= -g_{m_1}\left(\frac{1}{\lambda I_D}\Big\|\frac{1}{\lambda I_D}\right)$$

$$= \frac{1}{\lambda V_{eff_1}}$$

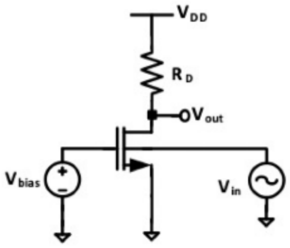
$$= -40\ V/V$$

3. It is possible to use the bulk terminal of a transistor as an input of an amplifier. Consider the single-stage NMOS amplifier shown below. For V_{bias}=1.5V:

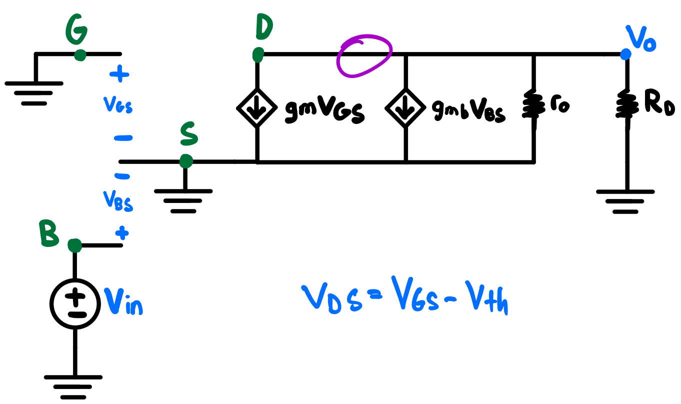
a) What is the region of operation of the transistor?

b) Calculate the small-signal gain ($A_v = V_{out}/V_{in}$) of the amplifier. **Recall** that $g_{mb} = \eta g_m$.

Assume, $\lambda = 0$, $\eta = 0.2$, $V_{TH(NMOS)} = 0.5V$, $\mu_n C_{ox} = 100\ \mu A/V^2$, $R_D = 1k\Omega$, $(W/L)_{NMOS} = 20$, and $V_{DD} = 3V$.



Small signal Model:



$V_{DS} = V_{GS} - V_{th}$

$V_{eff} = V_{GS} - |V_{th}| = 1.5 - 0 - 0.5 = 1V$

$g_{mb} = \eta g_m = \eta \mu_n C_{ox} \frac{W}{L} \cdot V_{eff}$

$= (0.2)(100\mu)(20)(1) = 0.0004$

$I_D = \frac{1}{2}(100\mu)(20)(1)^2 = 1mA$

$V_D = V_{DD} - I_D R_D = 3 - 1 = 2V$

$V_{DS} = 2 - 0 = 2V$

$V_{GS} - V_{th} = 1V$

$\rightarrow V_{DS} > V_{GS} - V_{th}$

KCL: $0 = g_{mb} V_{BS} + \frac{V_o}{R_D}$

$0 = (0.0004)(V_{in}) + \frac{V_o}{R_D}$

$-\frac{V_o}{R_D} = (0.0004)V_{in}$

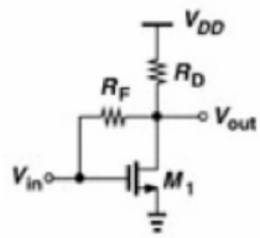
$\frac{V_o}{V_{in}} = -(0.0004)R_D$

$A_v = -0.4\ V/V$

SATURATION

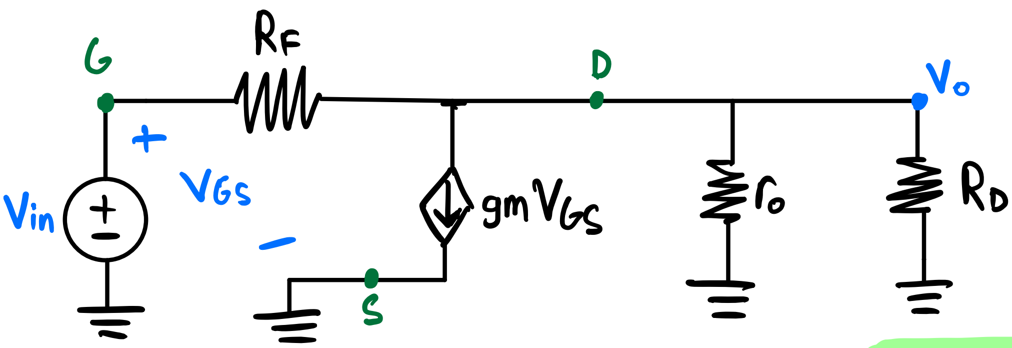
4. Note: In this problem you do not need to use any numerical value for the process parameters. If needed express your answers in terms of R_D, R_F and/or transistor small-signal parameters g_m and r_o.

In the following circuit, assuming the MOSFET is in active region:



a) Calculate the small-signal voltage gain (assume $\lambda \neq 0$).
b) Find the value of R_F for which the gain of the circuit is +1.
c) Find the value of R_F for which the gain of the circuit is -1.
d) State any condition that may be required so that the R_F calculated in part c is realizable.

Small Signal Model



a) $V_{in} = V_{GS}$

$$\frac{V_{in} - V_o}{R_F} = g_m V_{GS} + \frac{V_o}{r_o} + \frac{V_o}{R_D}$$

$$\frac{V_{in}}{R_F} - \frac{V_o}{R_F} = g_m V_{in} + \frac{V_o}{r_o} + \frac{V_o}{R_D}$$

$$\frac{V_o}{r_o} + \frac{V_o}{R_D} + \frac{V_o}{R_F} = \frac{V_{in}}{R_F} - g_m V_{in}$$

$$V_o\left(\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_F}\right) = V_{in}\left(\frac{1}{R_F} - g_m\right)$$

$$\therefore \frac{V_o}{V_{in}} = \frac{\left(\frac{1}{R_F} - g_m\right)}{\left(\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_F}\right)} = \boxed{\frac{R_D r_o - R_D R_F r_o g_m}{R_F r_o + R_D R_F + R_D r_o}}$$

b) $\boxed{R_F = 0\,\Omega}$

c) $\boxed{R_F = \dfrac{2 R_D r_o}{R_D r_o g_m - R_D - r_o}}$

d) $R_D r_o g_m - R_D - r_o > 0$

$$R_D r_o g_m > R_D + r_o$$

$$\boxed{g_m > \frac{R_D + r_o}{R_D r_o}}$$